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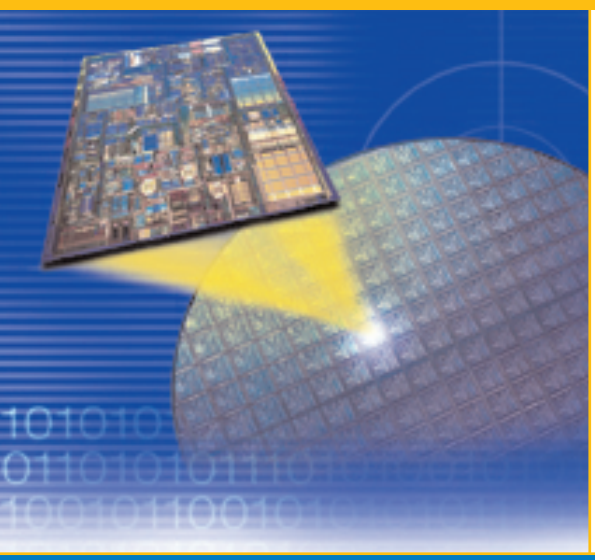

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Integration of Mixed-Signal Elements into a High-Performance Digital CMOS Process

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Integration of Mixed-Signal Elements into a High-Performance Digital CMOS Process

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ABSTRACT

The rapid increase in Internet communications' products such as high-speed switches, SerDes (serial-deserializer) elements and XAUI (X=10G, attachment unit interface) ports has energized the need for process technologies that support both digital and analog (mixed-signal) elements at radio frequencies (RF). In order for these products to be competitive, process technologies that support analog/mixed-signal and RF must heavily leverage the manufacturing benefits of conventional high-speed digital CMOS processes.

This paper reviews the challenges encountered when extending a high-speed conventional digital CMOS process to include analog/mixed-signal elements operating at RF frequencies.

INTRODUCTION

Analog/mixed-signal/RF product designs incorporating both CMOS and Bipolar Junction Transistor (BJT) active elements have emerged as a potential growth technology for the Internet communications marketplace.

Unlike older BiCMOS designs, these modern designs are adopting approaches where CMOS digital cells from well-characterized libraries are being mixed with specialized analog BiCMOS (or bipolar) modules. This enables rapid design modification, but places more demands on the process to deliver simultaneously optimized digital and analog elements [1].

Another key aspect of the analog/mixed-signal/RF process is the presence of passive elements. These passive elements include process-enabled elements (such as resistors and vertical capacitors) as well as design-enabled elements (such as inductors, varactors, and lateral capacitors).

SCALING CMOS (AND BICMOS) ACTIVE ELEMENTS

Digital CMOS has been successfully scaled for many generations and the performance optimization principles are well understood. Industry roadmaps such as the Semiconductor Industry Association (SIA) roadmap [2] and traditional industry scaling literature [3,4,5,6] reflect a long tradition of CMOS optimization.

In contrast, the optimization roadmap for analog/mixed-signal/RF is more difficult, due to conflicting digital and analog needs. The first problem is lack of commonality between digital and analog optimization strategies. The second problem is that desired analog process optimization strategies may run counter to traditional CMOS scaling, thus putting the extended analog/mixed-

signal/RF processes at odds with their mainstream CMOS progenitors.

The first problem (lack of commonality between digital and analog optimization priorities) can be more clearly illustrated by Tables 1 and 2. The tables represent an ordered list of CMOS DC parametrics and their importance in either analog or digital optimization. (The first item in each list is considered the most important.)

As just one example, note that I_{off} (of great priority to the digital designer) is not highly prioritized by the analog designer.

Table 1: Digital optimization strategy for DC parametrics

MOS - digital			
Parameter	Type	Units	Desired
Idsat	DC	mA/um	increase value
Ioff	DC	nA/um	decrease value
Vdd	DC	volts	decrease value
Vt	DC	mV	100mv < Vt < 300mV
Igate	DC	nA/um^2	decrease value

Table 2: Analog optimization strategy for DC parametrics

MOS - analog/RF			
Parameter	Type	Units	Desired
Vt	DC	mV	100mv < Vt < 300mV
gm	DC	uA/V	increase value
gds	DC	uA/V	decrease value
matching	DC	%	decrease differences
Igate	DC	nA/um^2	decrease value
Vcc	DC	volts	increase value
Ioff	DC	nA/um	decrease value

The second problem (desired analog process optimization strategies may run counter to traditional CMOS scaling) is becoming increasingly apparent in the literature. An illustrative example is I_{on}/I_{off} versus g_m/g_{ds}. Traditional CMOS scaling methodologies incorporate halo (pocket) implants to control short channel effects. However, halos have a detrimental effect on g_m/g_{ds} due to drain bias-induced modulation of the barrier created by the halo on the drain side of the device. This is a well-known problem and strategies ranging from lateral workfunction grading [7] to asymmetric halos [8] have been proposed. However, each of these strategies further removes the devices from the base technology, adding cost and complexity to the process.

Models and Measurements

A very critical part of process development is the ability to rapidly and precisely measure devices during the process development cycle and use these data to construct accurate and predictive device models. This creates both measurement and modeling challenges for the analog/mixed-signal/RF processes.

On the measurements side, although digital parts are well known to run at multi-GHz frequencies, CMOS digital optimization strategies do not require routine evaluation of RF metrics as part of process development. An analog/mixed-signal/RF process must enable such routine evaluation in order to produce accurate models at the 10+GHz of competitive products.

Since the digital community rarely evaluates RF metrics, the traditional metrics of the RF community become the metrics by default. These can be summarized as cut-off frequency (f_T), maximum oscillation frequency (f_{max}), minimum noise figure (NF_{min}) and noise figure at 50-ohm (NF_{50}), linearity (V_{IP3}), and 1/f noise level (usually shown as spectral noise density S_{vgate}) [1, 9,10].

Significant enhancements are required in CMOS measurement as well as in test chip design to support manual and automated RF measurements. More specifically, RF measurements require understanding and implementation of sophisticated de-embedding strategies [11]. RF devices are exceptionally sensitive to subtle differences in geometry [12], and test chip designs must incorporate significantly more device-specific calibration structures.

On the modeling side, circuit-level device models must clearly deliver accurate predictions at increasingly high frequencies. In addition, accurate simulators that enable noise figure calculation, noise parameter characterization (NF_{min}, G_{opt}, B_{opt}, and R_n) and time-domain noise simulation are indispensable to designers making trade-offs between power transfer and noise reduction [13].

Conventional compact models used in simulating digital circuits (e.g., BSIM3v3) lose accuracy at RF frequencies because the parasitic effects on high-frequency signals as they travel down the extrinsic region of the devices are ignored [14]. To accurately account for parasitic effects without over-burdening the circuit simulator, sub-circuit approaches employing lumped elements to represent device parasitics have gained popularity. These offer a good compromise between accuracy and speed [15].

In addition to parasitic effects, Non-Quasi-Static (NQS) effects become critical at higher frequencies, as the distributed RC effect inside the channel can no longer be ignored [16,17]. As the DC operating point in RF circuits moves from strong to weak inversion, an intrinsic MOSFET model that correctly models the turn-on of the transistor is essential. Furthermore, as oxide thickness aggressively scales to the direct-tunneling regime, the impact of gate leakage on device input impedance and minimum noise figure must be incorporated [18].

Substrate Noise Isolation

Digital CMOS devices are well known for the production of significant digital switching noise. CMOS digital circuits create short duration transients that generate both a continuous spectrum and a discrete spectrum (at multiples of the digital clock frequency). The clock harmonics are of particular importance in this marketplace because they may interact with the transmit/receive frequencies of communication elements.

Minimizing digital switching noise is a very difficult design issue [19]. Traditional noise-reduction methodologies include triple well (deep nwell), guard rings, careful attention to layout, and multiple voltage sources. In order to enhance the noise-isolation margin, noise-reduction strategies are frequently applied to both transmitters and receivers.

An interesting dilemma arises for higher frequency circuits (above 1GHz), where the advantages of many types of traditional noise isolation begin to fade. An example of this is provided in Figure 1, where simulation results are presented that compare triple well isolation and guard ring isolation as a function of frequency. Note that above 10GHz, the impact of traditional isolation methodologies is significantly reduced, and around 10GHz, methodologies such as guard rings offer equivalent benefits to triple well. In the <1GHz range, triple well on both the transmitters and receivers offers by far the best benefit.

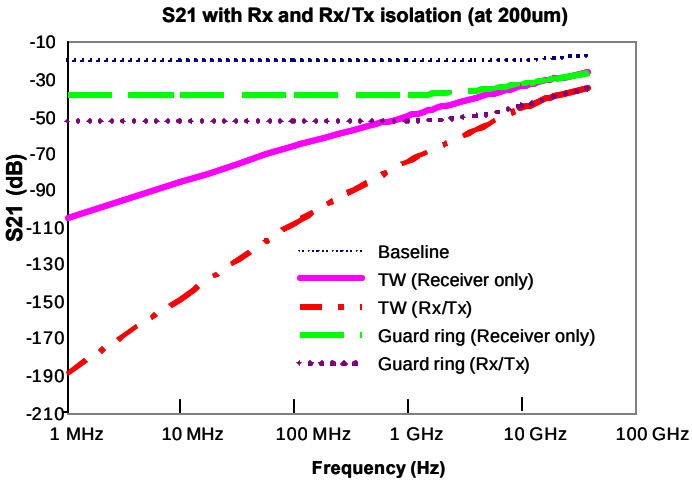

Figure 1: S_{21} noise isolation (in dB) comparing triple well to guard ring methodologies as a function of frequency

SiGe BJT DEVICES

SiGe epitaxial-base bipolar junction transistors are a key element in modern analog and high-frequency communications products. SiGe devices are the devices of choice for such applications as wireless Local Area Networks (LAN), 10G (with 40G on the horizon) synchronous optical networks (SONET) and in 1-2.5Gb/s Ethernet applications. SiGe devices also find application in the more traditional analog domain such as VCOs, mixers, power amplifiers, and Global Positioning Systems (GPS) devices.

The SiGe BJT is a richly researched device and only the high points will be covered here. Seminal review papers in 1995 and an update paper in 2001 provide an excellent summary of the field [20,21]. Table 3 summarizes key conference literature, indexed by company and performance level.

SiGe Performance Enhancement

The SiGe BJT provides performance enhancement in comparison with a conventional BJT device through three mechanisms.

The first enhancement arises from using the narrow SiGe bandgap to trade off against base and emitter implants. As can be seen in equation (1), decreasing the base bandgap energy (by adding Ge) permits an increase in base doping, which is desired, as it drops the base resistance, and a decrease in the emitter doping, which is also desired as it drops the emitter-base capacitance without seriously degrading . As can be seen from equations 2 and 3; lower R_b helps f_{max} and lower C_{eb} helps f_T. In addition (although not usually a limiter) the emitter transit time is inversely proportional to and thus benefits from the optimization.

$$\beta \propto \frac{N_{d(emitter)}}{N_{a(base)}} \times e^{\frac{E_{g(emitter)} - E_{g(base)}}{kT}} \quad (1)$$

$$f_T = \frac{1}{2\pi}\left[\frac{kT}{qI_c}\left(C_{eb}+C_{bc}\right)+\tau_b+\tau_e+\tau_{bc}\right]^{-1} \quad (2)$$

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_b C_{bc}}} \quad (3)$$

The second enhancement arises from tailoring the germanium profile (typically by ramping it across the rising edge of the base profile) in such a way as to accelerate electrons across the base and reduce the base transit time $\tau_b = W_B^2 / 2D_{nb}$.

Table 3: Comparison of key SiGe parameters as obtained from recent conference publications

Company	P. Author	FT	Fmax	Bvceo	Size	Alignment	Reference
Hitachi	K. Oda	124	174	2.3	0.2 x 1	SA	IEDM 2001
Conexant	M. Racanelli	170	160	2	0.15 x 10	SA	IEDM 2001
Infineon	J. Bock	106	145	2.3	0.18 x 2.8	SA	IEDM 2001
IHP	B. Heinemann	100	130	2.5	0.42 x 0.84		IEDM 2001
Hitachi	K. Washio	76	180	2.5	0.2 x 1	SA	IEDM 2000
ULSI	T. Hashimoto	73	61	2.6	0.15 x 6.15		IEDM 2000
Infineon	J. Bock	85	128	2.5	0.2 x 2.8	SA	IEDM 2000
Bell/Lucent	M. Carroll	58	102	3	0.28 x 0.84	SA	IEDM 2000
Infineon	J. Bock	52	65	2.7	0.2 x 0.28	SA	IEDM 1999
Hitachi	K. Washio	90	107	2	0.2 x 2	SA	IEDM 1999
IHP	K.E. Ehwald	55	90	2	0.8 x 2.5		IEDM 1999
Lucent	C.A. King	52	70	2	0.28 x 1.68	SA	IEDM 1999
IBM	G. Freeman	90	90	2.7	0.25 x 2.25	SA	IEDM 1999
Bell/Lucent	M. Carroll	45	35	4	0.28 x 1.68	SA	IEDM 1999
IHP	D. Knoll	65	90	2	1x1		IEDM 1998
IBM	Historic	90	90	2.7	A = 0.15 um^2		0.18 um
IBM	Historic	47	65	3.35	A = 0.3 um^2		0.25 um
IBM	Historic	47	65	3.35	A = 0.39 um^2		0.5 um

The third enhancement is an improvement in the Early voltage due to the use of a graded-Ge profile. The Early voltage is effectively a measure of how much the base profile can be depleted under reverse bias on the collector-base junction. Therefore, the Early voltage is a function of Ge-grading and reaches a maximum for a triangular Ge profile.

Self-Aligned SiGe BJT Devices

A typical SiGe BJT device incorporates a very thin SiGe layer wedged between the larger emitter and the substrate collector (see Figure 2). Presently, there are two common device configurations for modern SiGe BJT devices integrated into a BiCMOS process.

A quasi-aligned SiGe device (Figure 2, view "a") aligns the extrinsic base implant to the emitter poly edge. This means that "link" region (circled and a key contributor to R_b) is controlled by the interaction between two lithography layers (1 = the emitter cut and 2 = the emitter poly).

In contrast, the fully self-aligned device (Figure 2, view "b") uses a replacement emitter (usually called the emitter pedestal) and a spacer process to define the location of the extrinsic base implant. In this case, the extrinsic base is now "self-aligned" to the emitter as only one lithography operation (1 = emitter pedestal definition) is used to define the emitter cut and extrinsic base relationship.

The fully self-aligned device shows higher performance in the literature, but is somewhat more difficult to integrate due to the need to develop a replacement emitter process. As a consequence, the quasi-aligned process is frequently the more economical of the two.

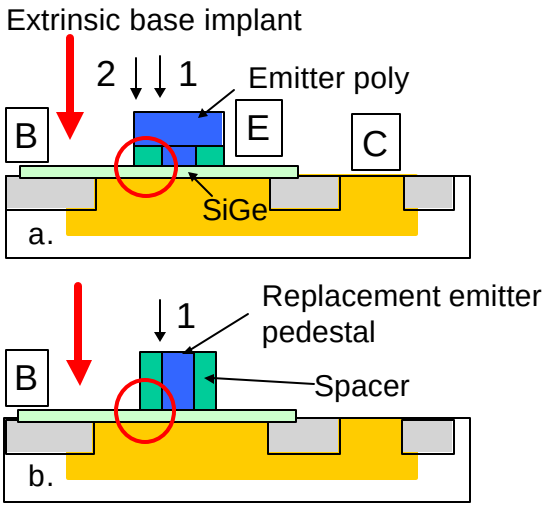

Figure 2: Comparison between quasi- and fully self-aligned SiGe bipolar transistor geometries

SiGe Versus CMOS

As the product marketplace moves to increasing integration of analog and mixed-signal elements with conventional digital CMOS, there are increasing demands on the process to economically integrate complex CMOS, BiCMOS, and bipolar process flows. With well-laid out CMOS devices showing f_T and f_{max} values in excess of 140GHz [12,22], a critical competitive question is "Why can't SiGe devices be replaced by CMOS?"

Table 4 attempts to answer this question by providing a high-level comparison between the key devices. CMOS devices offer the advantages of high f_T and f_{max} as well as superior linearity and lower voltage operation, due to lower threshold voltages (CMOS V_T in comparison to bipolar V_{BE}). BJT devices offer the advantages of excellent

noise performance and an improved transconductance (analog BJT in comparison to digitally-optimized CMOS). Also of interest in the comparison are density differences. BJT devices operating in low-noise amplifier applications occupy one-quarter to one- third the area of CMOS circuits of equivalent functionality. For the reverse example, CMOS devices operating in dense caches occupy one quarter to one third of the area of BJT circuits of equivalent functionality.

Note that noise is perhaps the major concern for CMOS RF design. The noise is due to the presence of interface states that introduce carrier trapping/de-trapping (1/f noise) and surface-roughness scattering (thermal noise). The coupling between the MOSFET channel and the gate also induces noise on the gate node at high frequencies.

Table 4: Comparison of CMOS with conventional and SiGe BJTs (summarized from Harame [1])

Parameter	CMOS	Si BJT	SiGe BJT
Ft	High	High	High
Fmax	High	High	High
Linearity	Best	Good	Better
Vbe (or VT) tracking	Poor	Good	Good
1/f noise	Poor	Good	Good
Broadband noise	Poor	Good	Good
Early voltage	Poor	OK	Good
transconductance	Poor	Good	Good

Designing Without BJT Devices

From a commercial CMOS perspective, the economical answer is to remove the BJT devices from the design. A SiGe BJT process adds between four and six masks to the conventional CMOS process, as well as a number of additional etches and thermal cycles that potentially damage the performance of the base CMOS devices. An ideal process would deliver SiGe performance using only CMOS.

Designing out the SiGe devices is an effort requiring both design and process contributions. From the design side, there is the requirement to design CMOS circuits that compensate for the poor noise performance. From the process side, there is the requirement to improve the analog performance of devices derived from a conventional digital process.

However, in the shorter term, the significant performance improvements offered by SiGe devices may validate the increased cost and complexity of integrating them into a full process flow.

PASSIVE ELEMENTS

A key difference between digital and mixed-signal processes is the presence of passive elements.

In the digital design world, performance is typically not determined by passive design elements. Capacitors are used as decoupling capacitors, and resistors are peripherally employed in IO-circuitry (in general, there are no intentionally fabricated inductors).

In strong contrast, in analog/mixed-signal design, performance is ultimately limited by the accuracy of the passive components in the technology [23,24,25,26,27]. In analog/mixed-signal design, passives (inductors, resistors, and capacitors) are used for a variety of active functions such as tuning, filtering, impedance matching, and gain control. Passives are key building blocks for circuits such as low offset voltage op-amps, analog frequency tuning circuits, switched capacitor circuits, filters, resonators, up-conversion and down-conversion mixers, VCOs, and D/A-A/D converters. The ability to accurately construct and model passives with Qs> 15-20 at frequencies >10G represents a key enabler for new circuits and products.

Inductors

Inductors are critical components in analog/mixed-signal design. Small-valued, precise, high-Q inductors are employed in circuits such as RF transceivers. Larger, lower-Q devices have functions such as impedance matching and gain control. Significant research has been done on monolithic integration of inductors, and in recent years there has been increasing use of inductors in state-of-the-art CMOS processes [28, 29, 30].

Spiral inductors in lengths can be fabricated with a conventional MOS process with negligible modifications to the design rules. A minimum of two metal layers is required, one to form the spiral and one to form the underpass. To minimize parasitic capacitance to the substrate, the top metal layer is the usual choice for the main spiral.

The most critical factor in inductor design is the optimization of the inductor Q at the design frequency. Q, or the "quality factor," is the ratio of the imaginary to the real part of the impedance (Q = Im(Z)/Re(Z)) and represents the ratio of the *useful magnetic stored energy* over the *average dissipation* for one cycle of the signal propagation. Note that determining the geometry and area required to deliver an optimized Q at the design frequency is not a straightforward process [31,32].

The most difficult factor in inductor process design is minimization of the impact of parasitic elements. Real inductors have parasitic resistance and capacitance. The parasitic resistance dissipates energy through ohmic loss, while the parasitic capacitance stores the unwanted energy. At high frequencies, the skin effect causes a non-

uniform current distribution in the metal segments, which introduces (among other things) a frequency-dependent contribution to the parasitic resistance. Finally, electromagnetic effects caused by the Faraday effect introduce parasitic currents (eddy currents) in the silicon as well, adding an additional frequency dependent term in the resistance [33].

Parasitic resistance is primarily driven by ohmic resistive losses in the thin patterned metal layers [34]. Parasitic resistance can be modulated both by design (trading off inductor area for inductor line width [35]) and by process (improving a Cu-damascene polish process to minimize dishing and thus permit wider metal lines).

Capacitive-induced loss is driven both by the Cox between the inductor and the substrate and by the lossy properties of the substrate. (At high frequencies the current flows through Cox and into the lossy substrate. The resulting dissipation adds a real component to the imaginary inductive impedance and degrades the Q.)

Minimizing this capacitance typically means separating the inductor as far as possible from the lossy silicon (usually by placing the inductor in the top metal layer). Recent advancements in low-k processes for digital CMOS also carry significant benefit (up to 4X improvement in Q for SiLK compared to conventional oxide ILD [35].)

Minimizing the substrate loss is more complex. As the frequency increases to where the skin depth is on the order of the substrate thickness, eddy currents in the substrate become a major loss mechanism. (This magnetically induced loss can be thought of as transformer action between a lossy primary and a lossy secondary [27].)

Mitigating eddy current loss can be quite difficult. There are a number of potential techniques including solid [33] and patterned ground shields [27], multilevel metalizations to build vertical solenoids [36], as well as minimizing doping levels under the inductor [33]. Note that since the eddy current loss is approximately proportional to the cube of the inductor diameter, strategies to minimize resistive parasitics by making large inductors (as is common in GaAs) are less effective in CMOS due to the more conductive Si substrates [27].

Capacitors

Analog/mixed-signal processes use four major types of capacitors. Polysilicon-insulator-polysilicon (PIP), metal-insulator-metal (MIM), lateral flux (finger), and MOS-style (depletion or accumulation).

Many older technologies have successfully used PIP capacitors. PIP capacitors do suffer from limited RF capability in the GHz range due to both the resistive losses in the plates and contacts, and to the parasitic capacitance between the passive element and the lossy silicon substrate [35]. Note also that the poly in PIP capacitors is typically implanted at higher doses than CMOS source-drain regions in order to minimize poly-depletion effects. This requires extra processing (and cost) because of additional lithography layers that need to be added to support the implants.

By far the most popular analog/mixed-signal capacitor is the metal-insulator-metal (MIM). MIM capacitors have the inherent advantage that they are metal (poly depletion and doping are non-issues) and, if implemented at the last metal layer, have the entire ILD stack between them and the substrate.

In recent years, the increasing interest in analog/mixed-signal commercial processes has led to implementation of MIM caps in commercial CMOS Cu-damascence processes [37,38,39]. The excellent linearity with voltage and temperature illustrates the popularity of the device as an analog element.

MIM devices are not without issues. Of special concern for today's processes is Cu metallurgy and its impact on yield and reliability. Also noteworthy is the choice of the inner layer dielectric. SiN is a popular choice due to common availability of the material in the traditional back-end process. However, note that low-temperature deposited SiN is known to show higher relaxation recovery voltages than oxide [40]. PECVD SiN displays significant sensitivity to operation frequency, bias voltage, and temperature when compared to oxide [41]. SiN also displays frequency dependent shifts that are consistent with bulk-nitride-traps [42] located within a tunneling distance of the nitride metal interface.

One of the restrictions with MIM devices is that process technologies do not scale the vertical spacing in the back end nearly as fast as the lateral spacing. The reason is that digital circuit designs cannot tolerate large increases in the wiring capacitance from generation to generation. Lateral flux (finger) capacitors solve this problem by using the lateral capacitance (between the metal lines) rather than the vertical capacitance (between the different ILD layers). As a consequence, the capacitance is under design control and scales more effectively with the technology [27].

Another of the limitations of the MIM device is the thickness of the insulator region. In contrast, MOS

devices can take advantage of thin gate oxide processes to achieve high capacitance per unit area. However, since one of the contacts is formed in silicon, the series resistance of a MOS capacitor is quite large. In addition, the very high gate leakage currents of modern scaled oxides (180 node and beyond, or <30A electrical) make gate-oxide-based MOS devices excessively leaky for conventional applications.

RESISTORS

Precision polysilicon and metal thin film resistors are key passive elements in analog circuits. The simultaneous presence of both poly and metal resistors can add value in a process, because the metal resistors are at the top of the stack and the poly resistors at the bottom. Two widely separated locations allow designers to chose a resistor that minimizes parasitics for their particular circuit. Also, the presence of a front-end resistor may enable in-line or early learning electrical evaluation on key circuit elements.

NAME	TYPE	Rho (ohm/sq)	VCR (ppm/V)	TCR (ppm/C)
Foundary A (N+)	N+ poly	126	-550	46
Foundary A (P+)	P+ poly	360	-56	-187
Foundary A HR	HR poly	1000	-70	-1250
Foundary B (N+)	N+ poly	77	210	46
Foundary B (P+)	P+ poly	258	519	148
Stuber (PS)	Polycide	12	320	440
Stuber (N+)	N+ poly	145	150	640
Stuber (P+) [45]	P+ poly	225	100	1440
Jeng #C (P+)	P+ poly	274		-96
Jeng #D (P+)	P+ poly	306		-285
Jeng #F (P+) [46]	P+ poly	244		-40

Table 5: Comparison of various poly resistors as reported by commercial sources and reviewed in the literature

Polysilicon Resistors

Polysilicon resistors exist in both silicided and unsilicided versions. Since the resistance of polysilicon-silicided (polycide) resistors tends to be quite low (5-15 ohms/sq), and the voltage coefficient tends to be quite high (100-600 ppm/V) there is a strong tendency to use the unsilicided (or silicide-blocked) resistors.

In a typical silicide-blocked resistor, the center of the device is silicide-blocked and the endcaps are left open. The endcaps either receive the conventional silicide processing for a contact pad, or receive optimized processing specific to the resistor application [43].

The silicide-blocking layer is usually an oxide or nitride and is frequently chosen to leverage a pre-existing layer elsewhere in the process. Existence of a silicide-blocking layer also enables devices such as silicide-blocked diffusion resistors (see Figure 3) and silicide-blocked MOS devices [44].

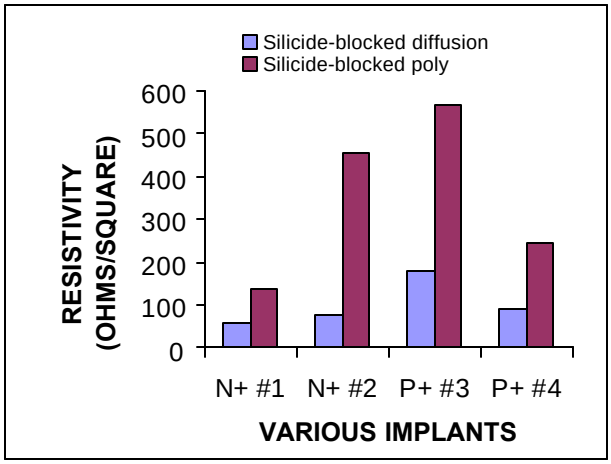

Figure 3: Resistivity for silicide-blocked diffusion and polysilicon resistors

Polysilicon resistors are usually placed on a field. In technologies with thin field oxides (such as LOCOS), there is significant electrical interaction through the field oxide and parasitic capacitance as well as depletion of the bottom of the resistor, which produces a voltage-dependent resistance change. All these must be considered in the resistor design [47]. Such effects are significantly reduced with the thicker oxides (3000-6000A), characteristic of STI processes, and they are also significantly reduced with SOI processing [48].

The sheet resistance, as well as the thermal and voltage coefficients of silicide-blocked polysilicon resistors, are very process-dependent. Implant conditions, grain boundary size, thermal activation, and end-cap silicide quality can all impact the key polysilicon resistor parameters. As a consequence, reported values for the major resistor parameters vary widely. Table 5 provides a cross-section of industry values, and Figure 3 compares values within a single Intel process for both silicide-blocked diffusion and poly devices.

Metal Film Resistors

Metal thin film resistors can be built at any of the traditional metal layers. In addition, a metal thin film resistor can be built as a by-product of the MIM capacitor

process. TaN is frequently used as well, due to its ready availability in a Cu-damascene process as a Cu-diffusion barrier. TaN is also interesting to the process designer as it exhibits a TCR-versus-resistivity relationship that ranges from roughly 500 ppm/C at 50 ohms/sq. to roughly (-)500 ppm/C at 400 ohms/sq and is attributed to the transition from metallic conduction (positive TCR) to hopping conduction (negative TCR). Zero TCR is ~250 ohms/sq. [39]. (A similar effect is also seen in W-silicide resistors, with a transition point at ~40 ohms/sq. [49].)

CONCLUSION

Analog/mixed-signal/RF continues to be a challenge for digital CMOS designers and manufacturers. Conflicting scaling methodologies, complex measurement and modeling support requirements, a multiplicity of interacting features, and increasingly complex process integration issues are the challenges to overcome to support the next generation of product designs.

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